IN THE CLAIMS:

Please cancel claims 21-35 as follows:

1. (Previously Presented) A hybrid built-in self test (BIST) architecture for embedded memory arrays that segments BIST functionality into remote lower-speed executable instructions and local higher-speed executable instructions, the architecture comprising:

a BIST logic controller that is separate from said embedded memory arrays, said BIST logic controller operates at a lower frequency than said embedded memory arrays and performs test functions common to all of said embedded memory arrays at said lower frequency; and

a plurality of blocks of test logic in communication with said BIST logic controller,

each one of said blocks is incorporated into a corresponding one of said embedded memory arrays under test,

said each one of said blocks operates at a same frequency as said corresponding one of said embedded memory arrays, said same frequency comprising a higher frequency relative to said frequency of said BIST logic controller,

said each one of said blocks performs test functions unique to said corresponding one of said embedded memory arrays at said same frequency,

said BIST logic controller further communicates, to said each one of said blocks of test logic, instructions at said lower frequency, and

said each one of said blocks further locally processes said instructions at said higher frequency.

2. (Previously Presented) The hybrid BIST architecture in claim 1, said each one of said blocks of test logic comprising a multiplier for increasing the frequency of said instructions from said lower frequency to said higher frequency.

3. (Previously Presented) The hybrid BIST architecture in claim 1, said each one of said blocks of test logic comprising:

a clock multiplier;

redundancy allocation logic;

data address control generation logic; and

decoding logic that decodes each of said instructions received from said BIST logic controller into multiple individual micro-instructions that are tailored to said corresponding one of said embedded memory arrays, and

said data address control generation logic and said redundancy allocation logic using said micro-instructions to perform data address control generation and redundancy allocation, respectively, based on said micro-instructions.

4. (Previously Presented) The hybrid BIST architecture in claim 1, said BIST logic controller in combination with said blocks of test logic enabling in parallel testing of at least one of the following:

different types of embedded memories, said different types comprising at least one of a dynamic random access memory (DRAM) array, a static random access memory (SRAM) array, and a content-addressable memory (CAM) array;

memory arrays operating at different frequencies; and

different size memory arrays.

5. (Previously Presented) The hybrid BIST architecture in claim 1, further comprising a lower-speed control bus operating at said lower frequency and connecting said BIST logic controller to said blocks so as to allow communication of said instructions from said BIST logic controller to said blocks.

6. (Previously Presented) The hybrid BIST architecture in claim 1, said BIST logic controller comprising at least one of a read only memory (ROM), a scannable read only memory (SROM), and other type of memory that stores macro instruction sets.

7. (Previously Presented) The hybrid BIST architecture in claim 1, said BIST logic controller comprising logic that provides branch prediction, program counter management, utility counters, and general BIST operation controls and diagnostic outputs.

8. (Previously Presented) A built-in self test (BIST) architecture for use with embedded memory arrays in functional circuitry within an integrated circuit, said BIST architecture comprising:

a BIST logic controller that is separate from said embedded memory arrays, said BIST logic controller operates at a lower frequency than said embedded memory arrays~~,~~ and performs test functions common to all of said embedded memory arrays at said lower frequency;

a plurality of blocks of test; and

a bus connecting said BIST logic controller to each one of said blocks of test logic so as to allow communication from said BIST logic controller to said blocks,

said bus operates at said lower frequency,

said each one of said blocks is incorporated into a corresponding one of said embedded memory arrays,

said each one of said blocks operates at a same frequency as said corresponding one of said embedded memory arrays, said same frequency comprising a higher frequency relative to said frequency of said BIST logic controller and said bus,

said each one of said blocks further performs test functions unique to said corresponding one of said embedded memory arrays,

said BIST logic controller ~~is~~ further communicates, to said each one of said blocks, instructions at said lower frequency via said bus, and

said each one of said blocks further locally processes said instructions at said higher frequency.

9. (Previously Presented) The BIST architecture in claim 8, said each one of said blocks of test logic comprising a multiplier for increasing the frequency of said instructions from said lower frequency to said higher frequency.

10. (Previously Presented) The BIST architecture in claim 11, said data address control generation logic and said redundancy allocation logic using said micro-instructions to perform data address control generation and redundancy allocation, respectively, based on said micro-instructions.

11. (Previously Presented) The BIST architecture in claim 8, said each one of said blocks of test logic comprising:

a clock multiplier;

redundancy allocation logic;

data address control generation logic; and

decoding logic that decodes each of said instructions received from said BIST logic controller into multiple individual micro-instructions that are tailored to said corresponding one of said embedded memory arrays.

12. (Previously Presented) The BIST architecture in claim 8, said BIST logic controller in combination with said blocks of test logic enabling in parallel testing of at least one of the following:

different types of embedded memories, said different types comprising at least one of a dynamic random access memory (DRAM) array, a static random access memory (SRAM) array, and a content-addressable memory (CAM) array;

memory arrays operating at different frequencies; and

different size memory arrays.

13. (Previously Presented) The BIST architecture in claim 8, said BIST logic controller comprising at least one of a read only memory (ROM), a scannable read only

memory (SROM), and other type of memory that stores macro instruction sets.

14. (Previously Presented) The BIST architecture in claim 8, said BIST logic controller comprising logic that provides branch prediction, program counter management, utility counters, and general BIST operation controls and diagnostic outputs.

15. (Previously Presented) A built-in self test (BIST) architecture for use with embedded memory arrays in functional circuitry within an integrated circuit, said BIST architecture comprising:

a BIST logic controller that is separate from said embedded memory arrays, said BIST logic controller operates at a lower frequency than said embedded memory arrays and performs test functions common to all of said embedded memory arrays at said lower frequency;

a plurality of blocks of test logic; and

a bus connecting said BIST logic controller to each one of said blocks of test logic so as to allow communication from said BIST logic controller to said blocks,

said bus operates at said lower frequency,

said each one of said blocks of test logic is incorporated into a corresponding one of said embedded memory arrays,

said each one of said blocks of test logic operates at a same frequency as said corresponding one of said embedded memory arrays, said same frequency is a higher frequency relative to said lower frequency of said BIST logic controller and said bus,

said each one of said blocks of test logic further performs test functions unique to said corresponding one of said embedded memory arrays,

said BIST logic controller ~~is~~ further communicates, to said each one of said blocks of test logic, instructions at said lower frequency via said bus,

said each one of said blocks of test logic further locally processes said instructions at said higher frequency, and

said test functions that are common to all of said embedded memory arrays comprise providing branch prediction, program counter management, utility counting, and general BIST operation control and diagnostic outputs.

16. (Previously Presented) The BIST architecture in claim 15, said each one of said blocks of test logic comprising a multiplier for increasing the frequency of said instructions from said lower frequency to said higher frequency.

17. (Previously Presented) The BIST architecture in claim 18, said data address control generation logic and said redundancy allocation logic using said micro-instructions to perform data address control generation and redundancy allocation, respectively, based on said micro-instructions.

18. (Previously Presented) The BIST architecture in claim 15, said each one of said blocks of test logic comprising:

a clock multiplier;

redundancy allocation logic;

data address control generation logic; and

decoding logic that decodes each of said instructions received from said BIST logic controller into multiple individual micro-instructions that are tailored to said corresponding one of said embedded memory arrays.

19. (Previously Presented) The BIST architecture in claim 15, said BIST logic controller in combination with said blocks of test logic enabling in parallel testing of at least one of the following:

different types of embedded memories, wherein said different types comprise at least one of a dynamic random access memory (DRAM) array, a static random access memory (SRAM) array, and a content-addressable memory (CAM) array;

memory arrays operating at different frequencies; and

different size memory arrays.

20. (Previously Presented) The BIST architecture in claim 15, said BIST logic controller comprising at least one of a read only memory (ROM), a scannable read only memory (SROM), and other type of memory that stores macro instruction sets.

21-35. (Cancelled).